MARKED-UP VERSION OF THE SPECIFICATION

GOVERNMENT CONTRACT

[0001] This invention has been developed with government support under U.S. Government Contract No. N00014-02-c-0473, awarded by the Office of Naval Research, Department of the Navy. The U. S. Government, therefore, has certain rights in this invention.

TECHNICAL FIELD

~~[0001]~~ [0002] This invention relates to an dry etching process for semiconductor substrates. More particularly, the present invention relates to a polymer dry etching process that produces smaller dimensionally accurate via holes for a thick polymer layer ~~in~~ on a semiconductor substrate while maintaining adjacent device features and reducing semiconductor wafer substrate cycle time through the reduction of processing steps.

BACKGROUND ART

~~[0002]~~ [0003] The current semiconductor ~~Semiconductor~~ technology [[is]] involves producing smaller device features, i.e., on the order of a micron and or a sub[[-]]micron. To accurately reproduce micron or sub[[-]]micron features, presently available dry etching processes need to be revised. The prior art etching process, using a photoresist mask for pattern transfer, results in limiting of the polymer etching depth, for example, forming a via-opening on a semiconductor substrate.

~~[0003]~~ [0004] Figures 1A and 1B are prior art etching process flow diagrams for creating a via-opening in a semiconductor substrate. As shown in Figure 1A, an insulating film 12 is deposited on a gallium arsenide (GaAs) semiconductor substrate 14. Afterwards, a first resist mask 16 is coated on the insulating film 12 and is patterned during exposure to ultraviolet light. Following this step, as shown in Figure 1B, the GaAs semiconductor substrate 14, including an insulating film 12 and a first resist layer 16, are etched, thereby removing the first resist mask 16, and thereby defining a via-opening 18. In this step, the thickness of the first resist mask 16 is limited by the present limitations of photoresist thickness technology, because a thicker resist mask, i.e., [[in]] on the order of several microns ~~range~~, will limit the minimum via hole feature size that can be accurately registered on a semiconductor substrate. In

addition, ~~because~~ since the selectivity of [[a]] the first resist mask 16 is poor ~~compared~~ relative to that of the insulating film 12, the polymer hole depth is limited in order to ~~keep~~ maintain an [[the]] aspect ratio (AR) of ~~the depth of the opening to the width of the opening~~ less than one, i.e., $AR = d^2/S < 1$, wherein d = the via depth, w = the via width, and wherein S = the via cross-sectional area or generally the width multiplied by the depth in a rectangular via. In other words, during the first etching ~~process~~ step of the prior art, ~~etching of~~ a polymer hole is formed having a depth being less than the width of the via-opening, thereby ~~will cause~~ causing a significant increase in the via hole width, thereby resulting in overlapping vias, and thereby damaging adjacent device features, such as resistors, capacitive layers, other via holes, or other transistor layers.

~~[0004]~~ **[0005]** Therefore, ~~it is extremely difficult to~~ etching the required polymer layer depth is extremely difficult in the prior art. As such, ~~it would be beneficial to~~ developing a new dry etching process would be beneficial to create deeper via holes, i.e., a few microns deep, for smaller width via-openings without ~~purchasing~~ requiring another exorbitant photoresist mask set ~~which may be expensive~~. Furthermore, for sub[[-]]micron-width vias, ~~there is~~ a need exists for increasing ~~to increase~~ the process margin for subsequent semiconductor processing steps. One method in the attempt to increase the process margin is ~~to create~~ creating a tapered via-opening for better metal-filling. Figure 1C is a prior art via structure showing a via hole before the step of hard mask removal. Figure 1D shows the prior art via structure after the step of hard mask removal. As shown in Figure 1D, the corners of insulating layer 21 are sharp and not tapered. As such, ~~there is~~ a need exists for a single via etching process that produces tapered sidewalls and removes the hard mask layer without the need for additional photoresist and wet chemical etching steps.

~~[0005]~~ **[0006]** In summary, ~~there is~~ a need exists for an improved etching process including an improved etching selectivity to achieve dimensionally accurate sub[[-]]micron via-openings and to provide other advantages over the prior art etching processes. Some of the other advantages include creating dimensionally accurate via holes and via hole sidewalls proximal to the top of a sub[[-]]micron via hole, and reducing wafer cycle time so that ~~there are~~ fewer steps are required ~~steps~~. Other advantages include creating an etching process that minimizes hazardous waste disposal issues, [[and]] that can be more precisely controlled or monitored by a semiconductor engineer, and that will be easier to transfer to production. Furthermore, this

needed process should produce greater process margin for sub[[-]]micron via holes, such as creating a tapered via-opening for subsequent processing steps. Still another advantage of this needed etching process is that the hard mask etch rate occurs at an extremely slow rate while the via-opening etch rate is extremely fast.

DISCLOSURE OF THE INVENTION

~~[0006]~~ **[0007]** Accordingly, the present invention provides an improved etching process for creating dimensionally accurate micron and sub[[-]]micron via-openings. ~~As disclosed, the~~ The present invention provides an improved via etching process that prevents adjacent devices from being etched. In [[one]] a first embodiment of the present invention, the etching process is utilized for via-hole processing. ~~As disclosed, the~~ The present invention is a via etching process for a polymer layer deposited on a semiconductor substrate, the process comprising the steps of depositing a polymer layer on the semiconductor substrate, depositing a hard-mask on the polymer layer, and depositing a photoresist mask on the hard-mask as well as a device thereby formed.

~~[0007]~~ **[0008]** In [[this]] the first embodiment, the first fluoride gas comprises trifluoromethane (CHF_3) and argon (Ar). The first fluoride gas comprises equal amounts of trifluoromethane (CHF_3) and argon (Ar). Additionally, ~~in this embodiment,~~ the hard-mask opening step further comprises applying bias power and pulse modulated power. The hard-mask opening step continues for a time duration in a range of three to five minutes. Afterwards, a second fluoride gas comprising ~~Sulfur Hexafluoride~~ sulphur hexafluoride (SF_6) and ~~Oxygen~~ oxygen (O_2) is released in the chamber to complete the creation of a vertical side wall via.

~~[0008]~~ **[0009]** In ~~another~~ a second embodiment of the present invention, a via etching process for a polymer layer on a semiconductor substrate ~~comprising~~ comprises the steps of[[:]] depositing a polymer layer defining a sub[[-]]micron wide via-opening on the semiconductor substrate[[,]] and depositing a hard-mask defining the sub-micron wide via-opening on the polymer layer. In this embodiment, performing a hard-mask removal and tapered via etching step, comprising[[:]] releasing a third fluoride gas into the chamber, whereby the hard-mask is etched away, and whereby an exposed portion of the polymer layer proximal to the sub-micron wide via-opening is etched away, to create tapered sidewalls. In the second

embodiment, the third fluoride gas comprises trifluoromethane (CHF_3) and argon (Ar). In yet one alternative of this embodiment, the third fluoride gas comprises equal amounts of trifluoromethane (CHF_3) and argon (Ar).

BRIEF DESCRIPTION OF THE DRAWINGS

~~[0009]~~ [0010] For a better understanding of the present invention, reference is made to the below-referenced accompanying drawings. Reference numbers refer to the same or equivalent parts of the present invention throughout the several figures of the drawings.

~~[0010]~~ [0011] Figure 1A is a section view of a prior art semiconductor structure.

~~[0011]~~ [0012] Figure 1B is a section view of a prior art semiconductor structure.

~~[0012]~~ [0013] Figure 1C is a section view of a prior art semiconductor structure.

~~[0013]~~ [0014] Figure 1D is a section view of a prior art semiconductor structure.

~~[0001]~~ [0002] Figure 2A is a section view of a semiconductor structure before the first etching step of the present invention.

~~[0015]~~ [0016] Figure 2B is a section view of a semiconductor structure after the first etching step of the present invention.

~~[0016]~~ [0017] Figure 2C is a section view of a semiconductor structure after the second etching step of the present invention.

~~[0017]~~ [0018] Figure 3 is a section view of the present invention of the semiconductor structure made by the first and second etching steps that create a via-opening in a polymer layer with vertical sidewalls.

~~[0018]~~ [0019] Figure 4A is a section view of a semiconductor structure, in accordance with [[of]] a second embodiment of the present invention, before the third etching step.

~~[0019]~~ [0020] Figure 4B is a section view of a semiconductor structure, in accordance with [[of]] a second embodiment of the present invention, after the third etching step.

~~[0020]~~ [0021] Figure 5 is a section view ~~of the present invention~~ of the semiconductor structure made using the third etching process that creates a tapered via-hole, in accordance with the present invention.

~~[0021]~~ [0022] Figure 6 is a flow chart of the polymer via etching process of the present invention.

MODES FOR CARRYING-OUT THE INVENTION

~~[0022]~~ **[0023]** The present invention is directed [[for]] to creating a via-opening within a semiconductor wafer. Accordingly, the present invention provides an improved etching process for creating dimensionally accurate micron and sub[[-]]micron via-openings. As disclosed, the present invention provides an improved via etching process that prevents adjacent devices from being etched. In one embodiment, the dry etching process is utilized for via hole processing.

~~[0023]~~ **[0024]** Figure 2A is a section view of a semiconductor structure before the first etching process of the present invention. In this Figure, a via etching layer structure is created by placing ~~in a chamber~~ (not shown in Figure) the semiconductor substrate 28 in a chamber. The semiconductor substrate 28 comprises a polymer layer 24 deposited thereon ~~on the semiconductor substrate 28~~, a hard-mask 30 deposited on the polymer layer 24, and a photoresist mask 32 deposited on the hard-mask 30.

~~[0024]~~ **[0025]** Figure 2B is a section view of a semiconductor structure after the first etching process of the present invention. The structure of Figure 2A is subjected to a [[A]] hard-mask opening process 34 ~~on the Figure 2A structure~~. During hard-mask opening process 34, a first fluoride gas is released into the chamber, whereby an exposed portion of the hard-mask 30, defining a via hole 26, is etched away. In the preferred embodiment, the chamber is a Trikon Omega 201™ Inductively Coupled Plasma (ICP) machine. In this embodiment, the first fluoride gas comprises equal amounts of trifluoromethane (CHF_3) and argon (Ar). The bias power is applied through a wafer chuck to the semiconductor structure. Preferably, the semiconductor structure is a semiconductor substrate. The hard mask ~~Hard-mask~~ opening process 34 further includes applying bias power, for a 4-inch radius semiconductor substrate, within a range of approximately 20 Watts to approximately 60 Watts and within a preferred range of approximately 25 Watts to approximately 32 Watts. For ~~other radius~~ semiconductor substrates of other radii, applied bias power is scaled ~~scales~~ to maintain the above described ratio of [[Watts]] power ranges to surface area of the semiconductor wafer. Afterwards, hard-mask opening process 34 further includes applying pulse-modulated power comprising inductively coupled plasma power from a machine such as Trikon Omega 201™ Inductively Coupled Plasma (ICP) machine. The applied pulse modulated power to the semiconductor substrate is within a range of approximately 450 Watts to approximately 900 Watts with a preferred range

of approximately 725 Watts to approximately 755 Watts. Additionally, the hard-mask opening process 34 includes pressurizing the chamber within a range of approximately 5 milli[[-]]Torr to approximately 20 milli[[-]]Torr with the preferred pressure of approximately 10 milli[[-]]Torr. To complete the first etching process, the hard-mask opening process 34 does all the above steps for approximately three to seven minutes.

~~[0025]~~ [0026] The Figure 2C is a ~~sideview~~ section view of a semiconductor structure resulting from performing a second etching process on the structure of Figure 2B ~~structure~~. During polymer etching process 40, a second fluoride gas is released into the chamber, whereby an exposed portion of the polymer layer 24 defining the via hole 26 is etched away, thus creating the via hole 26 with vertical sidewalls. The second ~~Second~~ fluoride gas comprises ~~Sulfur Hexafluoride~~ sulfur hexafluoride (SF_6) and ~~Oxygen~~ oxygen (O_2). Preferably, the second fluoride gas ~~comprising~~ comprises ~~Sulfur Hexafluoride~~ sulfur hexafluoride (SF_6) and ~~Oxygen~~ oxygen (O_2), wherein the volume ratio of gases is 1 part [[()]]SF_6[[()]] to 3 parts [[()]]O_2[[()]]. During the polymer layer etching process 40, [[a]] bias power and [[a]] pulse-modulated power are applied to the semiconductor substrate 28. Preferably, the polymer layer etching process 40 further includes applying bias power to a 4-inch radius semiconductor substrate within a range of approximately 40 Watts to approximately 100 Watts and with the preferred range of approximately 55 Watts to approximately 62 Watts. For ~~other radius~~ semiconductor substrates of other radii, applied bias power is scaled ~~scales~~ to maintain the above described ratio of [[Watts]] power ranges to surface area of the semiconductor wafer. Furthermore, preferably applying pulse-modulated power ~~comprising~~ comprises applying inductively coupled plasma power from an Trikon Omega 201™ ICP within a range of approximately 400 Watts to approximately 750 Watts and with the preferred range of approximately 475 to approximately 505 Watts. Finally, a polymer layer etching process 40 includes pressurizing the chamber the preferred range of approximately 1 milli[[-]]Torr to approximately 7 milli[[-]]Torr with the preferred pressure of approximately 5 milli[[-]]Torr. To complete the second etching process, the foregoing polymer layer etching process 40 steps ~~above~~ continues for approximately one and a half minutes to approximately six minutes.

~~[0026]~~ [0027] The addition of the first fluoride gas and the second fluoride gas to the chamber produces the unexpected results of achieving the vertical sidewalls for the via-hole of the present invention. In contrast, prior art etching processes utilizing only SF_6, i.e., the second

fluoride gas, did not achieve the present invention via-hole vertical sidewalls.

~~[0027]~~ **[0028]** In this embodiment, the hard-mask 30 is ~~Silicon Dioxide~~ silicon dioxide (SiO_2) and the polymer layer 24 is ~~Benzocyclobutene~~ a benzocyclobutene (BCB) polymer. In the alternative embodiment, the polymer layer 24 is a material with a dielectric constant less than 3 that etches at a rate greater than 10 times faster than that of the hard-mask. The semiconductor substrate is a compound material such as ~~Indium Phosphide~~ indium phosphide (InP), ~~Gallium Arsenide~~ gallium arsenide (GaAs), and a generally III-V semiconductor compound materials.

~~[0028]~~ **[0029]** Figure 3 is a section view of the present ~~inventive~~ invention structure have been subjected to the hard-mask opening process 34 and the polymer etching process 40. In this embodiment of the present invention, the hard-mask opening process includes ~~for approximately three to seven minutes~~ doing the following steps for approximately three to seven minutes ~~including~~: applying a first fluoride gas comprising an equal ratio of trifluoromethane (CHF_3) and argon (Ar) with an associated pressure of approximately 10 milli[[-]]Torr, applying a temperature of approximately 20 degrees C, applying pulse-modulated power, comprising inductively coupled plasma power, from a Trikon Omega 201™ ICP within a range of approximately 725 Watts to approximately 755 Watts, applying bias power ~~to the 4 inch radius semiconductor substrate~~ comprising a bias power with a range of approximately 25 Watts to approximately 32 Watts to the 4-inch radius semiconductor substrate, and completing the process within a range of approximately one and a half minutes to six minutes.

~~[0029]~~ **[0030]** In Figure 3, the via hole created has the following dimensions: a via-opening width 50 [[was]] of 1.66 microns (μm), a via depth 44 of 3.17 μm, the remainder after dry etch processing of a hard-mask 30 [[was]] of 0.44 μm, the distance 46 from the bottom of the via hole to the substrate [[is]] of 3.03 μm, and distance [[of]] to the bottom of the via hole 48 [[is]] of 1.32 μm. The via [[Via]] hole aspect ratio, i.e., ratio of the square of the via depth to cross-sectional area of the via-opening, i.e., the via width 50 multiplied by the via depth can be achieved within the preferred range of via depth to via width values greater than 4 to 1, i.e., where via-opening width 50 is 4 times smaller than the via depth 44. However, in an alternative embodiment of the present invention, a via-opening width 50 may selected within a preferred range of 0.4 μm to 2.0 μm, a via depth may be selected within a preferred range

of 2.0 μm to 6.0 μm, the remainder after dry etch processing of hard-mask 30 may be selected within a preferred range of 0.20 μm to 0.6 μm, a distance 46 from the bottom of the via hole to the substrate may be selected within a preferred range of 3.0 μm to 5.0 μm, and a distance of the bottom of the via hole 48 may be selected within a preferred range of 0.3 μm to 1.8 μm.

~~[0030]~~ [0031] Figure 4A is a section view of a semiconductor structure by the first and the second etching processes of the present invention before beginning the third etching process of the present invention. Initially, a semiconductor substrate 28 including a polymer layer 24 defining a sub[[-]]micron wide via-opening deposited on the semiconductor substrate 28, and a hard-mask 30 defining the sub-micron wide via-opening deposited on the polymer layer 24 is placed in a chamber.

~~[0031]~~ [0032] Figure 4B is a section view of a semiconductor structure after the third etching process of the present invention. During a hard-mask removal and a tapered via etching process 46, a third fluoride gas is released into the chamber, whereby hard-mask 30 is etched away, and whereby an exposed portion of polymer layer 24 proximal to the sub-micron wide via-opening is etched away to create tapered sidewalls. Third fluoride gas comprises trifluoromethane (CHF_3) and argon (Ar). Preferably, third fluoride gas comprises equal amounts of trifluoromethane (CHF_3) and argon (Ar). Afterwards, hard-mask and tapered via etching process 46 further includes applying bias power to a 4-inch semiconductor wafer within a range of approximately 60 Watts to approximately 200 Watts and with the preferred range of approximately 105 Watts to approximately 120 Watts, applying pulse-modulated power comprising inductively coupled plasma power from an ICP machine, such as Trikon Omega 201™ ICP, within a range of approximately 700 Watts to approximately 1000 Watts and with the preferred range of approximately 725 Watts to approximately 755 Watts. Further, pressurizing the chamber within a range of 5 milli[[-]]Torr to 20 milli[[-]]Torr with the preferred pressure of approximately 10 milli[[-]]Torr. The foregoing hard-mask ~~Hard-mask~~ and the tapered via etching process 46 ~~above mentioned~~ steps continue for approximately three to four minutes to complete the third etching process to achieve the hard-mask removal and the tapered via hole.

~~[0032]~~ [0033] The addition of the third fluoride gas for the third etching process to the chamber produces the unexpected results of allowing both the hard-mask removal and the

tapered via etch formation. In contrast, prior art wet etching process did not produce the tapered via hole of the present invention.

~~[0033]~~ **[0034]** Preferably, the hard-mask 30 is [[(]]SiO_2[[)]] and the polymer layer 24 is a benzocyclobutene (BCB) polymer. In the alternative, the polymer layer 24 is a material with a dielectric constant less than 3 and has an etch rate 10 times slower than that of the hard-mask 30. Furthermore, the ratio of the tapered sidewalls to non-tapered sidewalls is less than one-third. In this embodiment, the aspect ratio is greater than 1, i.e., the preferable ratio of the square of the via depth to the via cross-sectional area, i.e., the via depth multiplied by the via width, ~~of a depth of the via hole compared to the width of the via-opening~~ is a ratio greater than 2 to 1.

~~[0034]~~ **[0035]** Figure 5 is a section view of the third etching process. In this example, the hard-mask removal and the tapered via etching process 46 ~~includes for approximately three to four minutes~~ doing all the following steps for approximately three to four minutes: applying a third fluoride gas 47 comprising an equal ratio of trifluoromethane (CHF_3) and argon (Ar) with an associated pressure of approximately 10 milli[[-]]Torr, applying temperature of approximately 20 degrees C, applying pulse-modulated power comprising inductively coupled plasma power from an ICP machine, such as a Trikon Omega 201™ ICP, with the preferred range of approximately 725 Watts to approximately 755 Watts, and applying bias power within a preferred range of approximately 105 Watts to approximately 120 Watts.

~~[0035]~~ **[0036]** For this example, a sub[[-]]micron via-opening 54 is 1.0 μm, a depth 60 of 2.0 μm, the distance of bottom of the via hole 56 is 0.5 μm and the length of the tapered portion of via 58 is [[with]] in the approximate range of one-third to one-half the depth of the via 60. The via [[Via]] hole aspect ratios can be achieved within [[one]] a preferred range of via depth to via width values greater than 2 to 1, where via-opening width 54 may be 2 times smaller than the via depth 60. However, a via-opening width 54 may be within a preferred range of 0.80 μm to 1.20 μm; a via depth may be selected within a preferred range of 1.0 μm to 4.0 μm; and hard-mask 30 may be selected within a preferred range selected from 0.25 μm to 1.0 μm.

~~[0036]~~ **[0037]** Furthermore, the two via[[s]] processes may be used in series. For example, the process described in Figures 2A-3 may be performed ~~first~~ initially to produce vertical side wall via holes and the process described in Figures 4A and 4B may be performed secondly or

subsequently with the same chamber to produce a via hole which has generally vertical sides with some tapering proximal to the via-opening.

~~[0037]~~ **[0038]** Figure 6 is a flow chart for the present invention polymer etching process. In step 71, a hard mask 30 is deposited on [[said]] a polymer layer. In step 72, a photoresist mask is deposited on [[said]] a hard-mask 30. ~~In step~~ Step 73[[,]] comprises releasing a first fluoride gas into a chamber to etch a hard-mask opening for defining a via-hole opening. ~~Within~~ The step 73[[,]] also comprises applying pulse modulated power, bias power, temperature, and pressure, as described in paragraphs ~~[0023]~~ [0024] through ~~[0024]~~ [0025]. ~~In step~~ Step 74[[,]] comprises releasing a second fluoride gas into [[said]] the chamber to etch [[said]] the polymer layer defining [[said]] the via hole. ~~Within step~~ Step 74[[,]] comprises applying pulse modulated power, bias power, temperature, and pressure, as described above in paragraphs ~~[0025]~~ [0026] through ~~[0027]~~ [0028]. ~~In step~~ Step 75[[,]] comprises releasing a third fluoride gas into [[said]] the chamber for hard-mask removal and tapering. ~~Within step~~ Step 75[[,]] comprises applying pulse modulated power, bias power, temperature, and pressure, as described above in paragraphs ~~[0030]~~ [0031] through ~~[0033]~~ [0034].

~~[0038]~~ **[0039]** Information, as herein shown and described in detail, is fully capable of attaining the above-described object of the invention and the present embodiment of the invention, and is, thus, representative of the subject matter which is broadly contemplated by the present invention. The scope of the present invention fully encompasses other embodiments which may become obvious to those skilled in the art, and is to be limited, accordingly, by nothing other than the appended claims, wherein reference to an element in the singular is not intended to mean "one and only one" unless explicitly so stated, but rather "one or more." All structural and functional equivalents to the elements of the above-described embodiment and additional embodiments that are known to those of ordinary skill in the art are hereby expressly incorporated by reference and are intended to be encompassed by the present claims.

~~[0039]~~ **[0040]** Moreover, no requirement exists for a device or method to address each and every problem sought to be resolved by the present invention, for such to be encompassed by the present claims. Furthermore, no element, component, or method step in the present disclosure is intended to be dedicated to the public regardless of whether the element, component, or method step is explicitly recited in the claims. However, one skilled in the art

should recognize that various changes and modifications in form and material details may be made without departing from the spirit and scope of the inventiveness as set forth in the appended claims. No claim herein is to be construed under the provisions of 35 U.S.C. § 112, sixth paragraph, unless the element is expressly recited using the phrase "means for."

INDUSTRIAL APPLICABILITY

~~[0040]~~ **[0041]** The present invention applies industrially to a dry etching process for semiconductor substrates. More particularly, the present invention applies industrially to a polymer dry etching process that produces smaller dimensionally accurate via holes for a thick polymer layer [[in]] on a semiconductor substrate. ~~The process maintains adjacent device features and reduces semiconductor wafer substrate cycle time through the reduction of processing steps.~~